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ORIGINAL ARTICLE

Design of Energy Efficient 3GPP Turbo Encoder v5.0 Using High Range IO Standard Using Ultra Scale FPGA

Bhagwan Das[1], Abdul Aleem Jamali[1], M.R.Anjum[2], M.M. Shaikh[1]

[1,] Department of Electronic Engineering, Quaid-e-Awam University of Engineering, Science and Technology, Nawabshah, Pakistan
[2]Department of Electronic Engineering, The Islamia University of Bahawalpur, Pakistan

ABSTRACT

The 3GPP Turbo Encoder v5.0 offers the error correction and the high-speed data rate transmission for LTE at different high frequencies of operation. The execution of 3GPP Turbo Encoder v5.0 at high frequency of operation increases the on-chip temperature of the encoder. The increase in on-chip temperature of 3GPP Turbo Encoder v5.0 at high frequencies may permanently damage the device and interrupt in data communication. Currently, different techniques have been reported but significant on-chip temperature consumption is not reduced for the on-chip temperature of 3GPP Turbo Encoder v5.0. In this paper, the thermal efficient design for 3GPP Turbo Encoder v5.0 is achieved using IO Standard technique. The 3GPP Turbo Encoder v5.0 is operated with and without IO Standards for different frequencies of operation (i.e. 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz) via Ultra Scale FPGA. More than 60% on-chip temperature reduction is achieved for the designed 3GPP Turbo Encoder v5.0 using HR IO standard. The designed 3GPP Turbo Encoder v5.0 using HR IO Standard offers low on-chip temperature consumption for error-free data transmission.

Keywords: 3GPP Turbo Encoder, High Range IO Standard, Thermal efficient, Ultra Scale FPGA

Author`s Contribution
[1] Manuscript writing, Data Collection, Data analysis, interpretation, Conception, synthesis, planning of research
[2]Interpretation and discussion, Data Collection

Address of Correspondence
Bhagwan Das
Email: engr.bhagwandas@hotmail.com

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INTRODUCTION

The 3GPP Turbo Encoder v5.0 is a convolution encoder in Xilinx FPGA's core provides the error correction for 3GPP module communication for Multiplexing and Channel (Inc., 2015). The 3GPP Turbo Encoder v5.0 has block-based processing unit with the maximum input data bits of 5114 (Inc., 2015). The data block is handled via two Recursive Systematic Convolutional (RSC) encoders. These RSC encoders produce high-weight codes. The first RSC routes the input data and second RSC routes the interleaving of the input data. The reason for adopting this strategy is that if first RSC has a corrupted input bit then the second RSC will re-order the sequence. The delay is created in between first and second RSC's to generate block-aligned output (Pisek, Rajan, Abu-Surra, & Cleveland, 2017). The 3GPP Turbo Encoder v5.0 is specified with a rate of 1/3 turbo encoder using a single parity signal for each RSC[3, 4]. The 3GPP Turbo Encoder v5.0 can also be specified with a

rate of 1/5 turbo encoder for supplementary flexibility and error correction capability using two parity signals[5,6]. In this work, the 3GPP Turbo Encoder v5.0 is specified with a rate of 1/3 turbo encoder.

The performance of 3GPP Turbo Encoder v5.0 for XC3S50A–4 with the maximum data rate of 94.5 Mbps at 50 MHz channel bandwidth is reported in Xilinx Manual[1]. It is also discussed that 3GPP Turbo Encoder's temperature range for the standard operation in between -5°C to +150°C depends on the maximum data rate. It is further stated that 3GPP Turbo Encoder v5.0 is operated at different rates (i.e. 1/3 or 1/5). These rates of an encoder at the maximum data rate also vary the device temperature. The 3GPP Turbo Encoder v5.0 can be operated at core voltage ranging from 1.8 V to 3.0 V without IO Standard specification. It is discussed in (Das et al., 2017)[7], (Das et al., 2016)[8] and in (Ullah, I, 2018)[9] that different electronic devices due to increasing in device temperature may cause the permanent damage to the device. In this case, it is necessary to control the temperature variations for 3GPP Turbo Encoder v5.0. Several techniques are applied to control the temperature of electronic devices (such as, optical transmitter 10, 11, video decoders12, filters13). These techniques include; clock gating, voltage scaling, and variable frequency. However, each technique has its own advantages and disadvantages. It has been demonstrated in (Sharma, Khan, Das, Pandey, & Hussain, 2016)[14], (Das, Abdullah, Hussain, Pandey, & Verma, 2017)[15], (Saxena, Patel, & Khan, 2017)[16], and (Cai, X, 2018)[17] that variation in suitable IO Standard controls the temperature of the device. IO Standards are configured by changing the core voltage of FPGA.

In this paper, the thermal efficient design is demonstrated for 3GPP Turbo Encoder v5.0 using high range (HR) IO Standard via UFPGA. The HR IO Standard is selected based on the criteria of core voltage. HR I/O banks are designed to support a wider range of I/O standards with voltages of up to 3.3V. In the next, the 3GPP Turbo Encoder is designed using UFPGA to control the temperature of electronic devices at specified parameters.

RESEARCH METHODOLOGY

The UFPGA design of 3GPP Turbo Encoder v5.0 is developed via Xilinx Vivado with and without IO Standard. The temperature consumption is recorded for both with and without IO Standard designs. The methodology of the designed 3GPP Turbo Encoder v5.0 is shown in (Fig. 1).

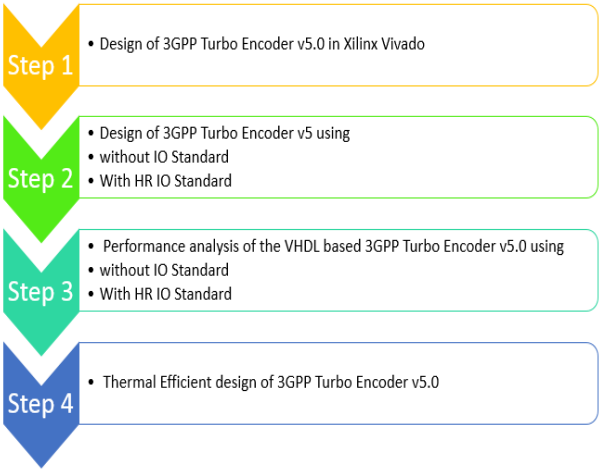

Fig. 1: Design steps for thermal efficient 3GPP Turbo Encoder v5.0

In the first design step, 3GPP Turbo Encoder v5.0 is developed in Vivado using VHDL coding by specifying different parameters. In the second design step, the VHDL based 3GPP Turbo Encoder v5.0 is configured with HR and without IO Standard. The HR IO Standard is selected based on the core voltage of FPGA and operating voltage of Encoder. In the third step, the designed Encoder is tested for different channel bandwidths (high frequencies) to analyze the thermal efficiency. Finally, the IO Standard based designed Encoder is implemented over UFPGA.

2.1. Design Step 1: VHDL based 3GPP Turbo Encoder v5.0

The 3GPP Turbo Encoder v5.0 is designed in Xilinx Vivado Suite using VHDL. The schematic design of VHDL based 3GPP Turbo Encoder v5.0 is shown in (Fig. 2).

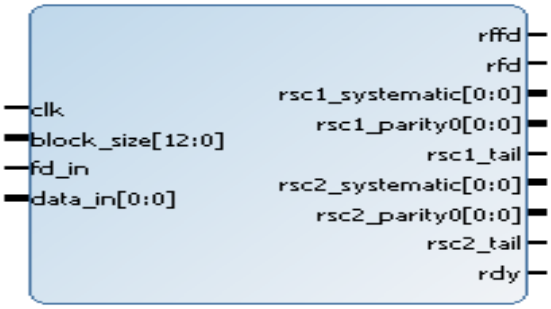

Fig. 2: Schematic design of VHDL based 3GPP Turbo Encoder v5.0

The VHDL based 3GPP Turbo Encoder v5.0 (in Fig. 2) is designed using different parameters as illustrated in Table 1.

Table 1: Parameters for 3GPP Turbo Encoder v5.0

Parameter	Value
Number of Channels	01
Coding rate	1/3
Memory Option	Internal
Address Generator	Internal
Address width	13

The VHDL based 3GPP Turbo Encoder v5.0 is configured using Clk pin for the clock signal that defines the synchronous operations at the rising edge of the clock signal. Block_Size pin addresses the width for current encode operation. fd_in pin, data_in pin, rffd pin, and rfd pin are used for the encoding process, data input, ready signal of first data, and core, respectively. rsc1_systematic pin is an output port from RSC1. rsc1_parity0 pin is for parity0 output from RSC1. rsc1_tail pin is used for the tail bits which is output on RSC1. Similarly, rsc2_systematic pin is an output port from RSC2. Rsc2_parity0 pin is for parity0 output from RSC2. rsc1_tail pin is for the tail bits that are being outputted on RSC2. rdy pin defines the valid data on the systematic and parity outputs.

It is discussed that the VHDL based 3GPP Turbo Encoder v5.0 is designed for 50 MHz channel bandwidth at the maximum data rate of 94.5 Mbps. The VHDL based 3GPP Turbo Encoder v5.0 discussed above is configured without IO Standard and ranges can be varied between -5°C to +150°C for different channel bandwidths. In the next, the VHDL based 3GPP Turbo Encoder v5.0 is designed using HR IO Standard.

2.2. VHDL based 3GPP Turbo Encoder v5.0 using HR IO Standard

The UltraScale FPGA consists of an I/O tile that has I/O buffer, I/O logic and I/O delay. Each IOB contains both input and output logic, and IO drivers. These drivers can be configured to various I/O standards, discussed in (Electronic Industry Alliance, 2017)[18], and (Xilinx Inc, 2016)[19]. The VHDL based 3GPP Turbo Encoder v5.0 is demonstrated using (Fig. 3).

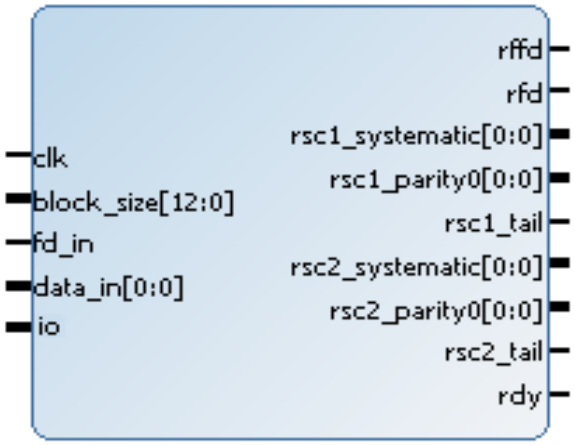

Fig. 3: Schematic design of VHDL based 3GPP Turbo Encoder v5.0 using HR IO Standard

It can be seen in (Fig. 3) that VHDL based 3GPP Turbo Encoder v5.0 IO Standard schematic diagram is different from the VHDL based 3GPP Turbo Encoder v5.0 without IO Standard. (Saxena et. al, 2017)[16] has listed many IO Standards supported by Virtex Ultra Scale FPGA. In this research, authors have selected the HR IO Standard that meets the requirements for the VHDL based 3GPP Turbo Encoder v5.0. These IO Standards are specified in the Electronic Industry Alliance JEDEC (Sharma, S, 2016)[14]. The reason for selecting the HR IO Standard is that it provides the core voltage of FPGA from 1.8 V to 3.3 V. Furthermore, HR IO Standard operates at high frequency operation of more than 100 MHz for many applications.

There are different types of HR IO Standards available such as; Low Voltage Transistor Transistor Logic (LVTTL), Low Voltage Complementary Metal-Oxide Semiconductor (LVCMOS), High-Speed Low-Voltage Digitally Controlled Impedance (HSLVDCI), and High-Speed Transceiver Logic (HSTL). These HR IO Standards suitable for VHDL based 3GPP Turbo Encoder v5.0 is selected to control the device temperature at high frequency operation and in this case, the LVCMOS is the most suitable choice. The LVCMOS has more temperature stability compared to other HR IO Standards at high frequency operation. In the next, the configuration of LVCMOS IO Standard based 3GPP Turbo Encoder v5.0is discussed.

1. **Low Voltage Complementary Metal-Oxide Semiconductor (LVCMOS)**

LVCMOS is a widely used IO Standard for 3.3V applications to maintain the temperature stability of the devices. UltraScale FPGA supports different LVCMOS IO Standard types such as; LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33. In this work, the LVCMOS33 IO Standard is used to match the core voltage of the FPGA with the operating voltage of the designed encoder. The syntax for changing the default IO Standard to LVCMOS:

a)

Attribute IOSTANDARD: string;

Attribute IOSTANDARD of IDIOA0: label is- "LVCMOS_33";

It was discussed earlier that the designed encoder has the bandwidth of 50 MHz with a temperature variation from -5°C to +150°C. In the next, thermal analysis for 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz is discussed for VHDL based 3GPP Turbo Encoder v5.0 with and without IO Standard.

3. Design Step 3: Thermal analysis of VHDL based 3GPP Turbo Encoder v5.0 with and without IO Standard

The thermal analysis is performed for designed Encoder at different frequencies with and without IO Standard.

3.1. Thermal analysis of VHDL based 3GPP Turbo Encoder v5.0 over different frequencies without IO Standard

The performance of the designed Turbo Encoder v5.0 is verified for 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz without using IO Standard. Table 2 illustrates the on-chip temperature measurements for the designed Turbo Encoder v5.0 without using IO Standard.

Table 2: Thermal Analysis for VHDL based 3GPP Turbo Encoder v5.0 without using IO Standard

Frequency Range for VHDL based 3GPP Turbo Encoder v5.0	The temperature of VHDL based 3GPP Turbo Encoder v5.0 without using IO Standard observed at a frequency in ºC
10 MHz	5ºC
20 MHz	11ºC
30 MHz	15ºC
40 MHz	19ºC
50 MHz	23ºC

The temperature measurements for the designed encoder without IO Standard are graphically demonstrated in (Fig. 4). It can be analyzed that at 10 MHz the temperature recorded is 5 ºC. For 20 MHz, the temperature of 11 ºC is observed. For 30 MHz, the temperature of 15 ºC is noted. For 40 MHz, the temperature of 19 ºC is recorded. Finally, for 50 MHz, the 23 ºC temperature is recorded.

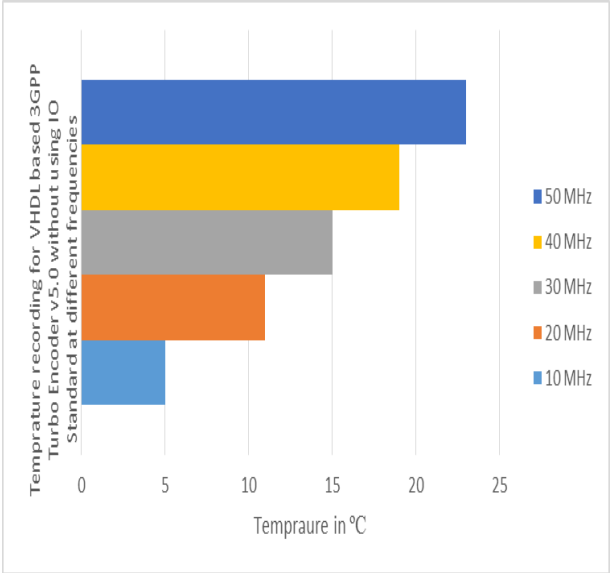

Fig. 4: On-Chip Temperature Analysis VHDL based 3GPP Turbo Encoder v5.0 without using IO Standard

It can be analyzed from (Fig. 4) that as the frequency of 3GPP Turbo Encoder v5.0 without using IO Standard is increased the temperature is also increased. It is determined that for 50 MHz the temperature recorded is 23ºC. These temperature measurements are practically not recommended. Furthermore, for other frequencies, the temperature is also more than the minimum device temperature that is -5ºC. In the next, the designed 3GPP Turbo Encoder v5.0 is designed using HR IO Standard is discussed.

3.2. Thermal Analysis of VHDL based 3GPP Turbo Encoder v5.0 over different frequencies using HR IO Standard

The performance of the designed 3GPP Turbo Encoder v5.0 is verified 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz using HR IO Standard. Table 3 illustrates the on-chip temperature measured at different frequencies for the designed 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard.

Table 3: Thermal Analysis for VHDL based 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard	
Frequency Range for VHDL based 3GPP Turbo Encoder v5.0	The temperature of VHDL based 3GPP Turbo Encoder v5.0 without using IO Standard observed at a frequency in ºC
10 MHz	-2ºC
20 MHz	0ºC
30 MHz	3ºC
40 MHz	7ºC
50 MHz	9.5ºC

The temperature measurements for the designed 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard are demonstrated in (Fig. 5). It can be analyzed from (Fig. 5) that as the frequency of the designed 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard is increased the temperature is also increased. However, the temperature measured is less in comparison to without IO Standard. It is observed that for 10 MHz, the temperature measured is -2ºC. Similarly, for 20 MHz, 30 MHz, 40 MHz, and 50 MHz, the temperature measurements are recorded as, 0ºC, 3ºC, 7ºC, and 9.5ºC respectively. It is important to note that temperature measurements for the designed 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard is less compared to without IO Standard.

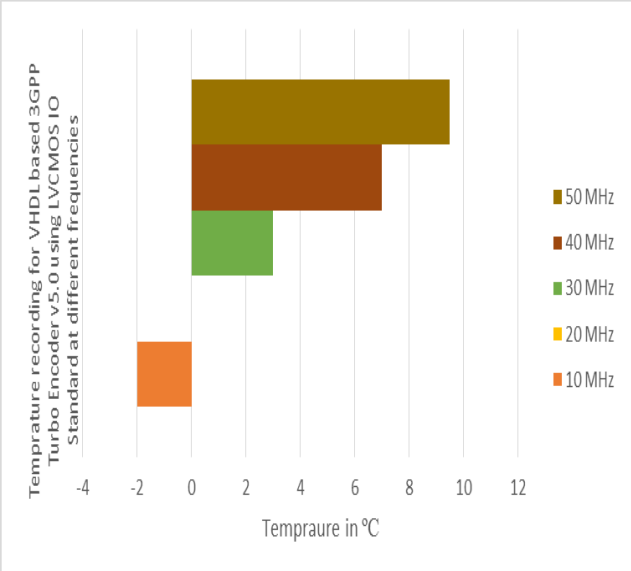

Fig. 5: On-Chip Temperature Analysis VHDL based 3GPP Turbo Encoder v5.0 using LVCMOS IO Standard

RESULTS & DISCUSSION

In this paper, the thermal efficient design of the designed 3GPP Turbo Encoder v5.0 is proposed using HR IO Standard. The HR IO Standard i.e LVCMOS IO Standard is selected according to the specification of 3GPP Turbo Encoder v5.0 and UltraScale FPGA. It is determined that the designed 3GPP Turbo Encoder v5.0 operates at the maximum frequency of 25 MHz and the operating voltage is more than 3V.

The temperature measurements observed at frequencies of 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz are 5ºC, 11ºC, 15ºC, 19ºC and 23ºC respectively for without IO Standard as shown in (Fig. 6). It is demonstrated that the designed HR (LVCMOS) IO Standard based 3GPP Turbo Encoder v5.0 is operated at frequencies 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz and the temperature recorded at these frequencies are -2ºC, 0ºC, 3ºC, 7ºC, and 9.5ºC respectively as depicted in (Fig. 6). It is demonstrated in (Fig. 6) that the HR IO Standard based 3GPP Turbo Encoder v5.0 operated at different frequencies has fewer temperature measurements compared to without IO Standard.

It is analyzed that the designed HR IO Standard based 3GPP Turbo Encoder v5.0 operated at 10 MHz has the temperature measurement of 5ºC and at same frequency without IO Standard the temperature measured is -2ºC. It is determined that 60% temperature reduction is achieved using HR IO Standard for the designed encoder compared to without IO Standard. For 20 MHz, using HR IO Standard the on-chip temperature consumption is reduced up to 89% compared to without using IO Standard for the designed encoder. For 30 MHz using HR IO Standard, the on-chip temperature consumption is reduced up to 80% compared to without using IO Standard for the designed encoder. For 40 MHz using HR IO Standard, the on-chip temperature consumption is reduced up to 63% compared to without using IO Standard for the designed encoder. Finally, at 50 MHz using HR IO Standard the on-chip temperature consumption is reduced up to 58% for the designed encoder. The HR IO Standard based design of 3GPP Turbo Encoder v5.0 provides the rapid signal termination and has less leakage current compared to without using IO Standard.

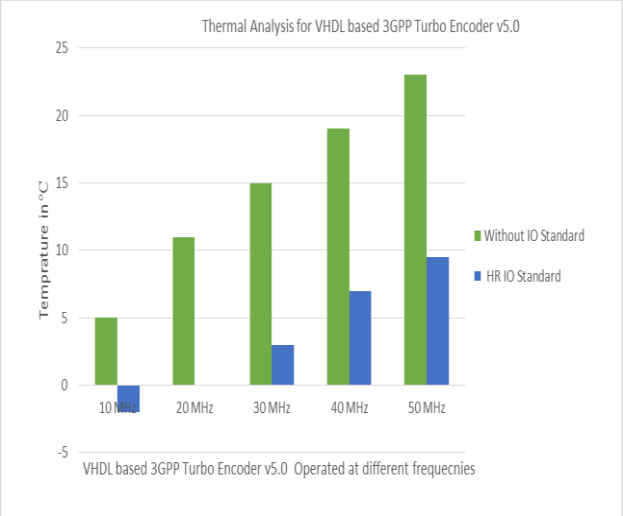

Fig. 6: Thermal Analysis for of VHDL based 3GPP Turbo Encoder v5.0 using without IO Standard and HR IO Standard

It is also observed that the designed 3GPP Turbo Encoder v5.0 using HR IO Standard operated at different frequencies has similar core voltage of UltraScale FPGA (i.e. 3.3 V). Due to this, leakage current and on-chip temperature are very low for different frequencies compared to without IO Standard. According to (Inc., 2015)1 and (Wang, Li, & Ting, 2017)20 the temperature recorded for existing encoder is from 25ºC to 50ºC, which is practically high and in real-time not feasible for data transmission. It has been demonstrated that the designed HR IO Standard based 3GPP Turbo Encoder v5.0 has minimum temperature measurements of -2ºC to 9.5ºC at high frequency operation compared to existing work. The designed Encoder using HR IO Standard offers error free data transmission for existing high frequency LTE system.

CONCLUSION

The thermal efficient design of 3GPP Turbo Encoder v5.0 using HR IO Standard is achieved. The designed 3GPP Turbo Encoder v5.0 is operated at different frequencies with and without IO Standard. It is determined that temperature reduction is achieved with HR IO Standard in comparison to without IO Standard. The temperature for 10 MHz, 20 MHz, 30 MHz, 40 MHz, and 50 MHz are reduced to 89%, 89%, 80%, 68% and 58%, respectively. It is concluded that the designed 3GPP Turbo Encoder v5.0 using HR IO Standard offers low on-chip temperature measurements for high operating frequencies.

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